Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of processing an instruction, said method comprising:

fetching said instruction using a corresponding address from a memory unit, wherein a first ~~plurality of possible~~ meaning~~s are~~ is associated with said instruction stored at said corresponding address by a same processor when a first plurality of bits from said corresponding address is concatenated with said instruction, and wherein a second meaning is associated with said instruction stored at said corresponding address by said same processor when a second plurality of bits from said corresponding address is concatenated with said instruction;

concatenating a portion of said corresponding address to said instruction to form an extended instruction, ~~wherein selection of said portion of said corresponding address for said concatenating is independent of region of said memory unit from which said instruction is fetched, and~~ wherein said concatenation increases a number of instructions in an instruction set; and

executing said extended instruction, wherein said portion of said corresponding address determines a meaning for said extended instruction from said possible meanings.

2. (original) The method as recited in Claim 1 wherein said portion is an address bit.

3. (original) The method as recited in Claim 1 wherein said portion is a plurality of address bits.

4. (original) The method as recited in Claim 1 wherein said plurality of possible meanings include an integer type of instruction and a floating point type of instruction.

5. (currently amended) A method of handling an instruction, said method comprising:

generating said instruction, wherein a ~~plurality of possible~~ first meaning~~s~~ ~~are~~ is associated with said instruction stored at a corresponding address by a same processor when a first plurality of bits from said corresponding address is concatenated with said instruction, and wherein a second meaning is associated with said instruction stored at said corresponding address by said same

processor when a second plurality of bits from said corresponding address is concatenated with said instruction;

storing said instruction at a particular address in a memory unit such that a portion of said particular address enables determination of a meaning for said instruction from said possible meanings; and

before executing said instruction, fetching said instruction using said particular address from a memory unit and concatenating said portion of said particular address to said instruction, ~~wherein selection of said portion of said particular address for said concatenating is independent of region of said memory unit from which said instruction is fetched, and~~ wherein said concatenation increases a number of instructions in an instruction set.

6. (original) The method as recited in Claim 5 wherein said portion is an address bit.

7. (original) The method as recited in Claim 5 wherein said portion is a plurality of address bits.

8. (original) The method as recited in Claim 5 wherein said plurality of possible meanings include an integer type of instruction and a floating point type of instruction.

9. (original) The method as recited in Claim 5 wherein said generating said instruction and said storing said instruction are performed by a compiler.

10. (currently amended) A system comprising:

a memory unit for storing a plurality of instructions at a plurality of addresses; and

a processor operable to fetch a particular instruction from said memory unit by providing a corresponding address, wherein a first ~~plurality of possible~~ meaning~~s are~~ is associated with said particular instruction stored at said corresponding address by a same processor when a first plurality of bits from said corresponding address is concatenated with said particular instruction, and wherein a second meaning is associated with said particular instruction stored at said corresponding address by said same processor when a second plurality of bits from said corresponding address is concatenated with said particular instruction, and wherein said processor is operable to concatenate a portion of said corresponding address to said particular instruction to determine a meaning for said particular instruction from said possible meanings before executing said particular instruction, ~~wherein selection of said portion of said corresponding address for said concatenation is independent of region of said memory unit from which said instruction is fetched, and~~ wherein said concatenation increases a number of instructions in an instruction set.

11. (original) The system as recited in Claim 10 wherein said portion is an address bit.

12. (original) The system as recited in Claim 10 wherein said portion is a plurality of address bits.

13. (original) The system as recited in Claim 10 wherein said plurality of possible meanings include an integer type of instruction and a floating point type of instruction.

14. (original) The system as recited in Claim 10 further comprising a compiler for generating said plurality of instructions and for storing each instruction at an appropriate address in said memory unit.